## REMARKS

Claims 1, 4-14, and 16-29 are pending in this application. Claims 2, 3, and 15 have been canceled by a previous amendment. In the Final Office Action, claims 1, 4-14, and 16-29 are rejected over prior art. Reconsideration of the rejection is respectfully requested.

### RESPONSE TO ARGUMENTS

In response to Applicants' remarks filed on August 08, 2006, the Examiner opines that Horisaki et al. teaches an "integrated" burn-in test program for testing a multi-chip package having multiple kinds of semiconductor devices including at least two of a non-volatile memory (NVM), a SRAM, and a DRAM, as recited in claims 1, 4, 8, 12 and 21-22.

Initially, Applicants wish to clarify the term a "multi-chip package having multiple kinds of semiconductor devices," recited in the claims. As illustrated in FIG. 3 and the disclosure on paragraphs [0038-0039], a single multi-chip package may contain more than two memory devices, for example, NVM, DRAM, and SRAM. The multi-chip package is not a single semiconductor device package, which may be an individual NVM, DRAM, or SRAM.

Paragraph [003] of Horisaki et al. clearly teaches that a problem of the prior art's burn-in test equipment is that it **cannot** generate test patterns when **different** semiconductor memories are tested because **different** semiconductor memories such as DRAM and SRAM have different number of I/O pins. In other words, although burn-in test equipment may test first memories having a first number of I/O pins, when second memories having a second number of I/O pins are loaded onto the burn-in test equipment, the burn-in test equipment cannot generate new test pattern for the newly loaded second memories. More specifically, the prior art's burn-in test

equipment may test a DRAM, but cannot test a SRAM because the number of I/O pins are different for the DRAM and the SRAM.

It appears, the Examiner has failed to fully appreciate the term "multi-chip package having multiple kinds of semiconductor devices," or, the Examiner mistakenly believes that "integrated" burn-in test program, recited in the claims, means any test that can test more than one memory device. However, even if the term "plural test conditions" used in Horisaki et al. is broadly interpreted to mean "integrated," Horisaki et al. only teaches that the "integrated" test program is able to process first memories having a first number of I/O pins and second memories having a second number of I/O pins. In otherwords, two or more batches of individual semiconductor devices (NVA, DRAM, or SRAM) may be tested back to back by the burn-in equipment. Horisaki et al. teaches testing semiconductor memories (individual NVA, DRAM, or SRAM) with different number of different I/O pins. Accordingly, Horisaki et al. fails to teach each and every feature of claims 1, 4, 8, 12 and 21-22.

The Examiner also opines that the Bardsley et al. reference teaches uploading an integrated burn-in test program, because Bardsley et al. teaches using "IBM's ES/9000 mainframe computer and uses pseudo-random pattern generator which generates a test pattern for BIST of MCM." (Emphasis added.)

However, as the Examiner may know, built-in-self-test (BIST) is an integrated circuit that is part of the MCM, i.e., integrated into the semiconductor memory package. Bardsley et al. specifically teaches that the "pseudo-random pattern generator is packaged on the MCM." In other words, the BIST and pseudo-random pattern generator are part of the MCM, and not that

the IBM's ES/9000 mainframe computer uploads an integrated burn-in test program to test multi-chip packages having at least two of NVA, DRAM, and SRAM.

Accordingly, Bardslet et al. fails to teach each and every feature of claims 1, 14, 21, and 27.

**CLAIM REJECTION UNDER 35 U.S.C. §103**

Claims 1, 4-6, 8-13, 21-26 and 28 are rejected under 35 U.S.C. § 102(b) as being unpatentable over Applicants admitted prior art (APA) and in view of by Horisaki et al. (JP 2001-155497). The rejection is respectfully traversed.

With regard to independent claims 1 and 21, the Examiner alleges that the APA teaches "multi-chip package having multiple kinds of semiconductor devices" and "the multiple kinds of semiconductor devices include at least two of a non-volatile memory, a SRAM, and a DRAM." The Examiner further alleges that the APA fails to teach "uploading an integrated burn-in test program," but the Examiner alleges that Horisaki et al. teaches such a feature.

The Examiner has clearly made the classical mistake of combining elements of several references without taking into consideration the relationship and function of each elements or steps recited in the claims, and the effects of such combination. For example, claim 1 recites testing multiple kinds of semiconductor devices including at least two of a non-volatile memory (NVM), a SRAM, and a DRAM. Claim 1 further recites "uploading an integrated burn-in test program," and "the integrated burn-in test program is adapted to test the non-volatile memory, the SRAM, and the DRAM." (Emphasis added.)

As remarked above, paragraph [003] of Horisaki et al. clearly teaches that a problem of the prior art's burn-in test equipment is that it **cannot** generate test patterns when **different** semiconductor memories are tested because **different** semiconductor memories such as DRAM and SRAM have different number of I/O pins. In other words, although burn-in test equipment may test first memories having a first number of I/O pins, when second memories having a second number of I/O pins are loaded onto the burn-in test equipment, the burn-in test equipment cannot generate new test pattern for the newly loaded second memories. Applicants submit that multi-chip packages having at least two of NVA, DRAM, and SRAM, as recited in claim 1, would have the same number of I/O pins. Therefore, "integrated burn-in test program" recited in the claims means a program that can test more than one type of memory; whereas, "integrated program," in Horisaki et al. at best teaches an integrated burn-in test program for semiconductor memories having different number of I/O pins. No where in Horisaki et al. does it teach that the burn-in test equipment can test multiple kinds of semiconductor devices including at least two of a non-volatile memory (NVM), a SRAM, and a DRAM, recited in the claims. Therefore, Horisaki et al. also cannot teach "uploading an integrated burn-in test program," and "the integrated burn-in test program is adapted to test the non-volatile memory, the SRAM, and the DRAM." (Emphasis added.)

Accordingly, a combination of the APA and Horisaki et al. would still fail to teach all the features of claims 1 and 21. For at least the reasons given above, claims 1 and 21 are patentable over the Examiner's cited references. Dependent claims 4-6, 8-13, 22-26, and 28 are also patentable for respectively depending on an allowable base claim.

Claims 1, 14, 16-18, 20-21, 27 and 29 are rejected under 35 USC 103(a) as being unpatentable over Applicants admitted prior art (APA) in view of Bardsley et al. (MCM BURN-N EXPEREINCE). The rejection is respectfully traversed.

With regard to independent claims 1, 14, 21 and 27, the Examiner alleges that the APA teaches "multi-chip package having multiple kinds of semiconductor devices" and "the multiple kinds of semiconductor devices include at least two of a non-volatile memory, a SRAM, and a DRAM." The Examiner further alleges that the APA fails to teach "uploading an integrated burn-in test program," but the Examiner alleges that Bardsley et al. teaches such a feature.

Claim 1 recites "uploading an integrated burn-in test program," and "the integrated burn-in test program is adapted to test the non-volatile memory, the SRAM, and the DRAM." (Emphasis added.)

As remarked above, Bardsley et al. teaches a MCM having BIST with a pseudo-random pattern generator. In other words, the BIST and the pseudo-random pattern generator are integrated **into** the MCM. Since the pseudo-random generator generates a test pattern, and the pseudo-random generator is part of the BIST, which is integrated into the MCM, then Bardsley et al. cannot teach "uploading an integrated burn-in test program to burn-in equipment," as recited in claims 1, 14, 21 and 27. In other words, there is **no program** for the IBM ES/9000 mainframe computer to upload. In fact, there is no program. A test pattern is not an integrated burn-in test program. The only "program" taught in Barsley et al. is "the defect isolation software," which isolates chip failure in the logic block.

For at least the reasons given above, claims 1, 14, 21 and 27 are patentable over the Examiner's cited references. In addition, dependent claims 16-18, 20, and 29 are also patentable for respectively depending on an allowable base claim.

Claims 7 and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Horisaki et al. in view of APA in further view of Eide (U.S. Patent 6,014,316). This rejection is also respectfully traversed.

As discussed above, Horisaki et al. neither suggest nor teaches the features recited in independent claims 1 and 14. In addition, the APA nor Eide cure the deficiencies of Horisaki et al. Therefore, respective dependent claims 7 and 19 are also patentable for depending on respective allowable base claim.

## CONCLUSION

In view of the above remarks, reconsideration of the rejections and allowance of claims 1, 4-14 and 16-29 are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below. If the Examiner believes that a personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (703) 668-8000.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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